63. The memory control hub of claim 62, wherein said request packet includes a field indicating if a completion packet is required in response to the respective request packet.

64. The memory control hub of claim 63, wherein arbitration between said hubs is symmetric and distributed.

65. The memory control hub of claim 64, wherein a hub is allotted ownership of said interface up to a predetermined amount of time.

66. The memory control hub of claim 50, wherein the memory control hub and a processor are integrated on a single semiconductor unit.

67. The memory control hub of claim 50, wherein the memory control hub and a graphics unit are integrated on a single semiconductor unit.

REMARKS

The following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

Title

The title has been amended to as requested by the examiner. The title has been replaced with the following title: "Method and Apparatus For an Improved Interface Between A Memory Control Hub and An Input/Output Control Hub".

35 U.S.C. § 102(e) Rejections

Examiner rejected claims 1, 2, 4-20, 22-35, and 37-67 as being anticipated by U.S. Patent No. 6,088,370 (hereinafter referred to as Bell).

> "To anticipate a claims, the reference must teach every element of the claim. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (Manual of Patent Examining Procedures (MPEP) ¶ 2131.)

Independent claims 1, 16, 29, 30, 47, and 50 of the present application includes limitations not disclosed or taught by the Bell. As a result, the independent claims 1, 16, 29, 30, 47, and 50 are not anticipated by the Bell.

In particular, the independent claims include the limitation of an interface "between a memory control hub (MCH) and a input/output control hub (ICH)".

Bell, however, does not disclose an interface between a memory control hub (MCH) and a input/output control hub (ICH). Rather, Bell only discloses a bus system that provides "connections between a controller 115, which functions as a bridge between a microprocessor bus 110, to which one or more microprocess devices are connected . . . and bus expander bridges 117, 120, and 125." (Bell Col. 2, lns. 21-27).

Considering Bell does not disclose an interface between a memory control hub (MCH) and a input/output control hub (ICH), as is claimed by applicant, Bell does not anticipate applicants independent claims.

In addition, applicants' remaining claims depend from at least one of the independent claims mentioned above. As a result of depending from one of the independent claim, the remaining claims include the distinguishing limitations discussed above, and are therefore also not anticipated by Bell.

CONCLUSION

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call John Ward at (408) 720-8300.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

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